Paper 50

Power Proportional Adder Design for the Internet of Things in a 65 nm Process

Adrian Wheeldon, Jordan Morris, Danil Sokolov, Alex Yakovlev

Power Proportional Adder Design for IoT

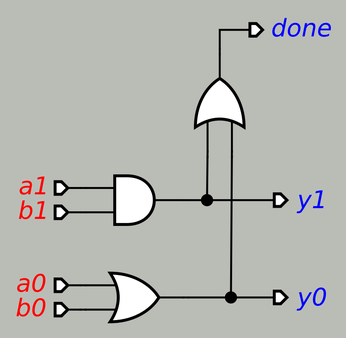
Adrian Wheeldon a.r.wheeldon2@ncl.ac.uk
μSystems Group, Newcastle University, UK

Motivation

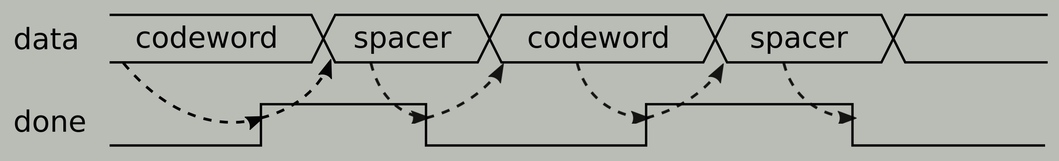
- Adapt performance to delay variations.
  - Unstable power supply (maximum power point tracking).
    - Voltage can drop very low (subthreshold).
    - Rather do work slowly, rather than no work at all.
    - Voltage can vary widely—solar, wind.
  - Supply variation due to battery drain.
  - Process variation—especially in subthreshold.
  - Environmental temperature changes.
- Supply-driven energy consumption and performance.
  - Dynamic voltage/frequency scaling set at design time.
  - Can we adapt to runtime conditions?
- Based on 65 nm commercial low-power process.
  - Good perfomance/leakage trade-off for Internet of Things.

How does self-timing work?

- No clock signal.
  - Local handshaking.
  - Still has some timing assumptions.
- Each data bit represented by two wires.
  - Codewords separated by *spacers*.
  - Codewords are $\{0,1\}$ or $\{1,0\}$.
  - Spacers are $\{0,0\}$ or $\{1,1\}$.
  - Remaining combination is forbidden.

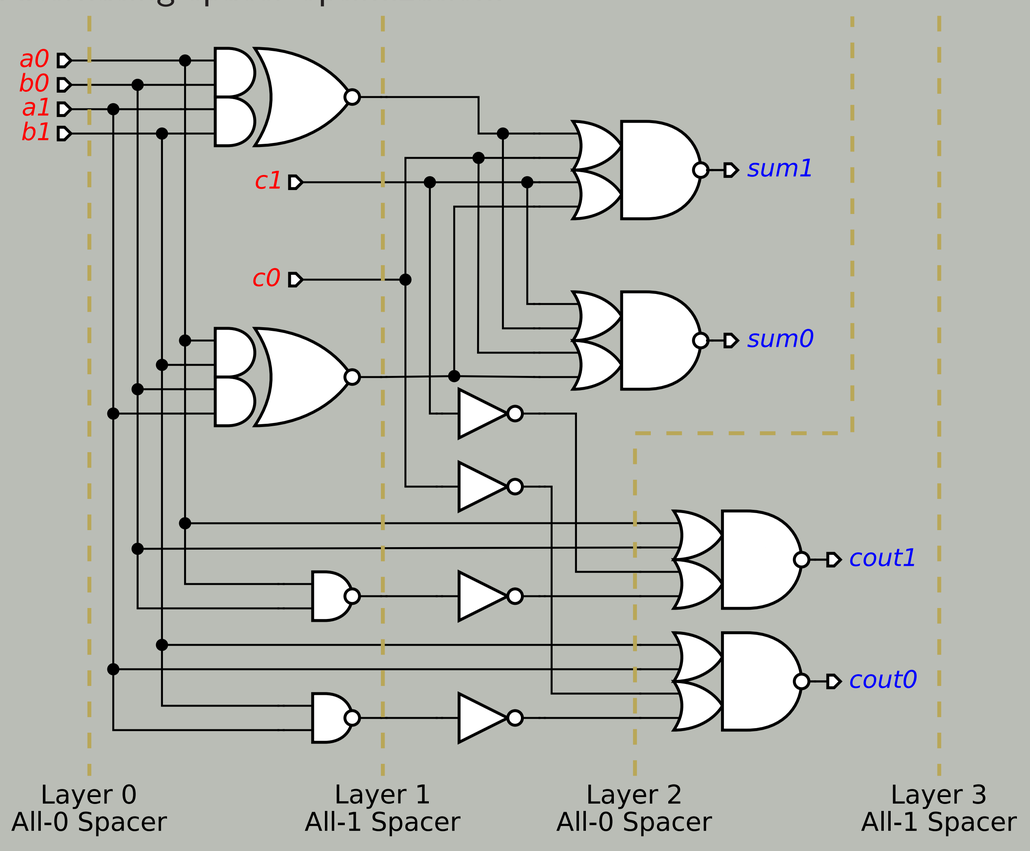


Dual-rail AND gate with completion detection.



Solution

- Dual-rail asynchronous design.
  - Self-timed based on actual runtime delays.
  - Completion detection notifies on finished computation.
  - Performance is always average-case.
- Alternating spacer optimization.



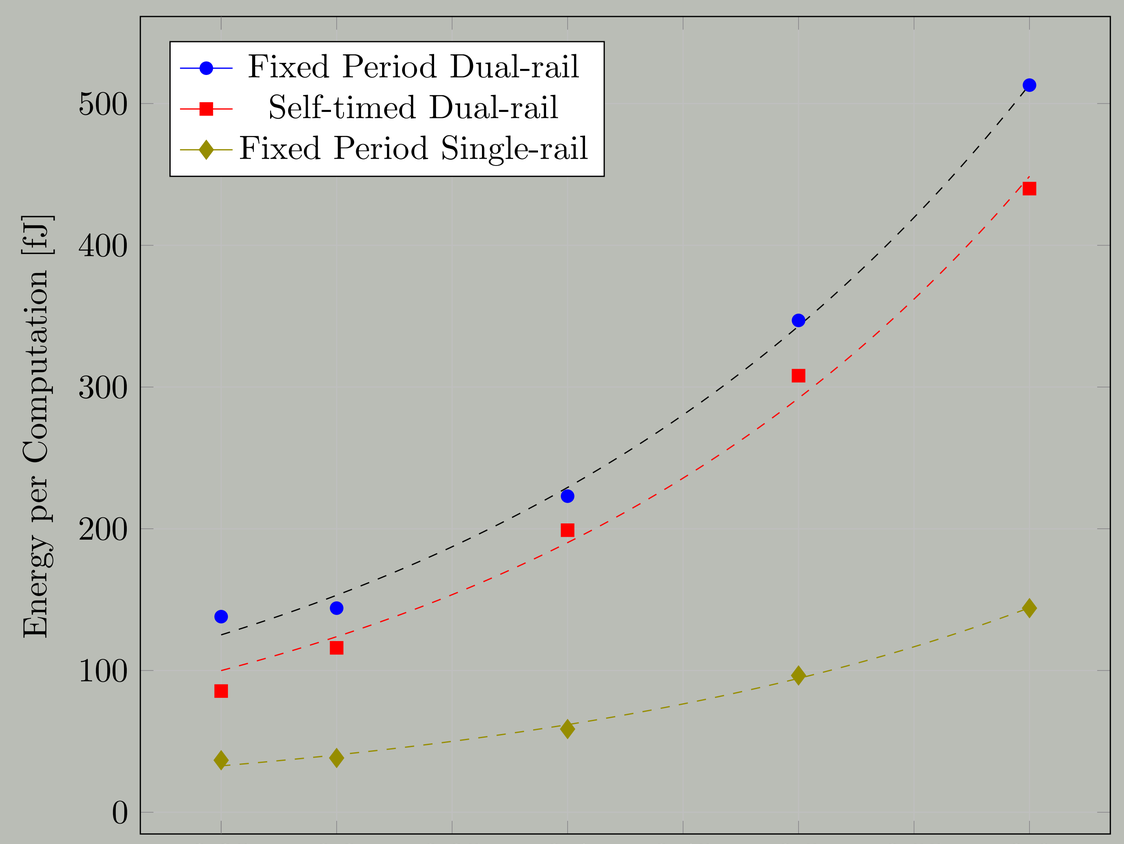
Cell Library[*]

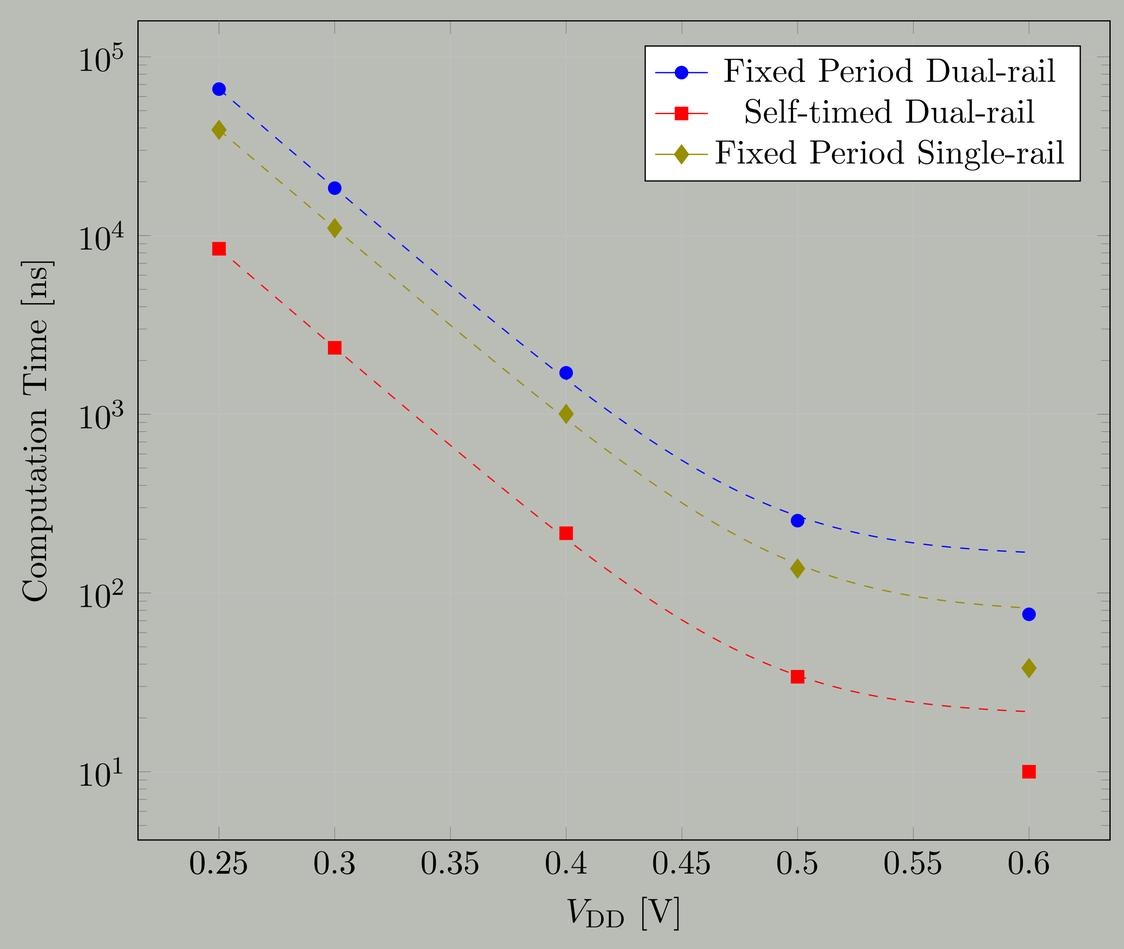
- High performance optimized for subthreshold.
- Faster than competing libraries at the same supply voltage.
  - Can we use less energy by dissipating more power for less time?

[*] J. Morris et al., "Unconventional Layout Techniques for a High Performance, Low Variability Subthreshold Standard Cell Library," in Proc. ISVLSI 2017.

Results

- Simulation results from addition of 130 000 operands.





Conclusion

- The design operates with elastic timing.
  - Across a wide supply voltage.
  - Robust to process, voltage and temperature variations.
- Can we use a dual-rail circuit in single-rail mode?
  - Bring average energy per computation closer to single-rail.